National Semiconductor

October 15, 2008

DS91M040
125 MHz Quad M-LVDS Transceiver

General Description

The DS91M040 is a quad M-LVDS transceiver designed for driving / receiving clock or data signals to / from up to four multipoint networks.

M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs. M-LVDS devices also have a very large input common mode voltage range for additional noise margin in heavily loaded and noisy backplane environments.

A single DS91M040 channel is a half-duplex transceiver that accepts LVTTL/LVCMOS signals at the driver inputs and converts them to differential M-LVDS signal levels. The receiver inputs accept low voltage differential signals (LVDS, BLVDS, M-LVDS, LVPECL and CML) and convert them to 3V LVCMOS signals. The DS91M040 supports both M-LVDS type 1 and type 2 receiver inputs.

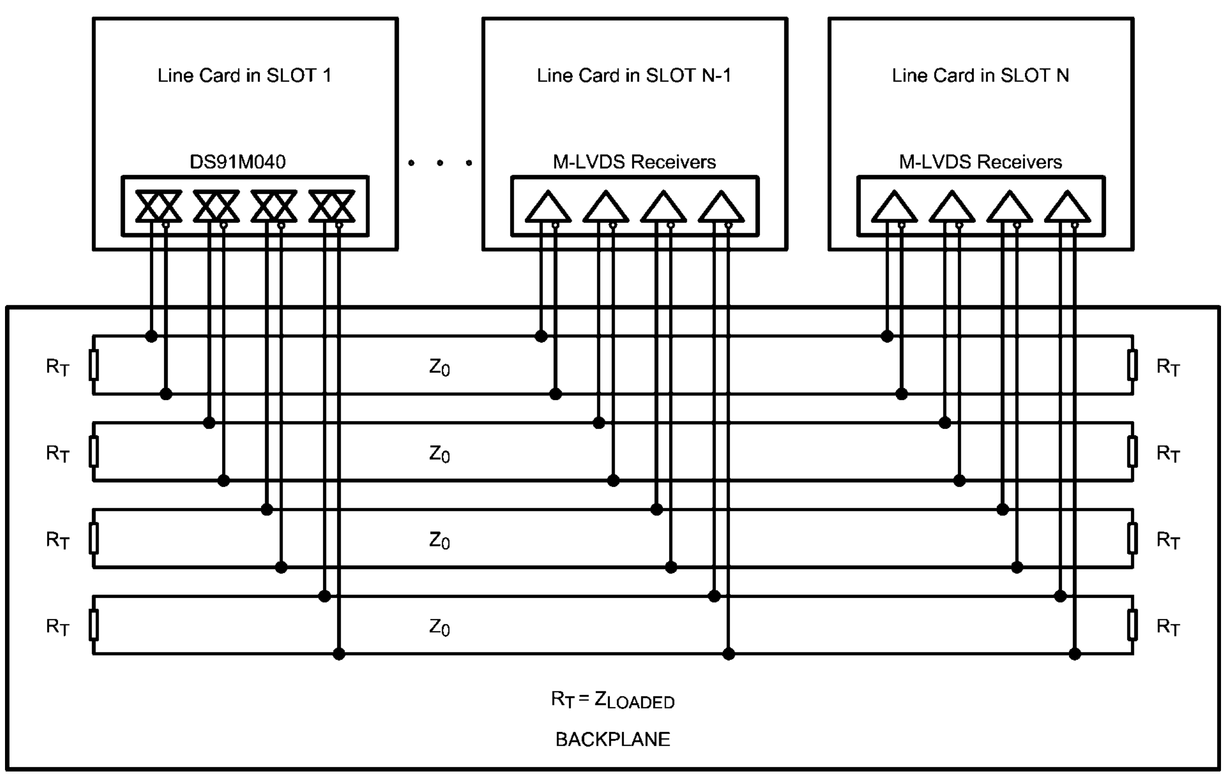
Features

- DC - 125 MHz / 250 Mbps low jitter, low skew, low power operation
- Wide Input Common Mode Voltage Range allows up to ±1V of GND noise
- Conforms to TIA/EIA-899 M-LVDS Standard
- Pin selectable M-LVDS receiver type (1 or 2)
- Controlled transition times (2.0 ns typ) minimize reflections
- 8 kV ESD on M-LVDS I/O pins protects adjoining components
- Flow-through pinout simplifies PCB layout
- Small 5 mm x 5 mm LLP-32 space saving package

Applications

- Multidrop / Multipoint clock and data distribution
- High-Speed, Low Power, Short-Reach alternative to TIA/EIA-485/422
- Clock distribution in AdvancedTCA (ATCA) and MicroTCA (µTCA, uTCA) backplanes

Typical Application



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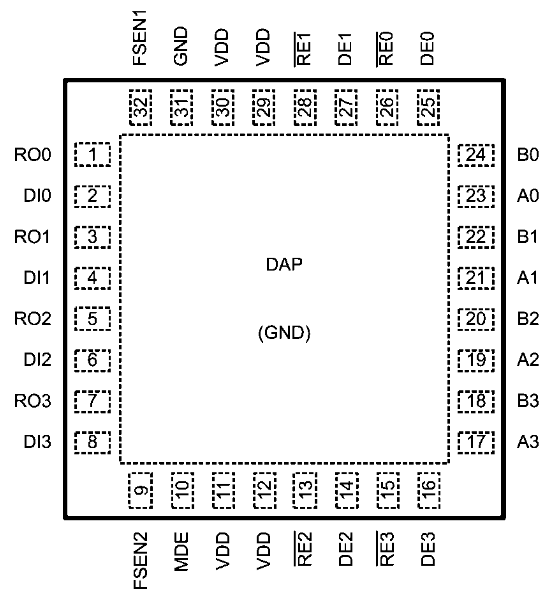
Ordering Information

Order Number	Receiver Input	Function	Package Type
DS91M040TSQ	Type 1 or 2	Quad M-LVDS Transciever	LLP-32

Connection Diagram



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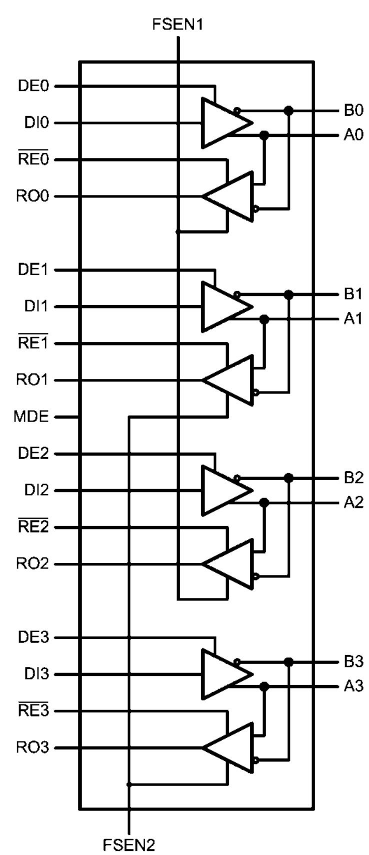
Logic Diagram



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Pin Descriptions

Number	Name	I/O, Type	Description
1, 3, 5, 7	RO	O, LVCMOS	Receiver output pin.
26, 28, 13, 15	$\overline{RE}$	I, LVCMOS	Receiver enable pin: When $\overline{RE}$ is high, the receiver is disabled. When $\overline{RE}$ is low, the receiver is enabled. There is a 300 kΩ pullup resistor on this pin.
25, 27, 14, 16	DE	I, LVCMOS	Driver enable pin: When DE is low, the driver is disabled. When DE is high, the driver is enabled. There is a 300 kΩ pulldown resistor on this pin.
2, 4, 6, 8	DI	I, LVCMOS	Driver input pin.
31, DAP	GND	Power	Ground pin and pad.
17, 19, 21, 23	A	I/O, M-LVDS	Non-inverting driver output pin/Non-inverting receiver input pin
18, 20, 22, 24	B	I/O, M-LVDS	Inverting driver output pin/Inverting receiver input pin
11, 12, 29, 30	V_{DD}	Power	Power supply pin, +3.3V ± 0.3V
32	FSEN1	I, LVCMOS	Failsafe enable pin with a 300 kΩ pullup resistor. This pin enables Type 2 receiver on inputs 0 and 2. FSEN1 = L --> Type 1 receiver inputs FSEN1 = H --> Type 2 receiver inputs
9	FSEN2	I, LVCMOS	Failsafe enable pin with a 300 kΩ pullup resistor. This pin enables Type 2 receiver on inputs 1 and 3. FSEN2 = L --> Type 1 receiver inputs FSEN2 = H --> Type 2 receiver inputs
10	MDE	I, LVCMOS	Master enable pin. When MDE is H, the device is powered up. When MDE is L, the device overrides all other control and powers down.

M-LVDS Receiver Types

The EIA/TIA-899 M-LVDS standard specifies two different types of receiver input stages. A type 1 receiver has a conventional threshold that is centered at the midpoint of the input amplitude, $V_{ID}/2$. A type 2 receiver has a built in offset that is 100mV greater then $V_{ID}/2$. The type 2 receiver offset acts as a failsafe circuit where open or short circuits at the input will always result in the output stage being driven to a low logic state.

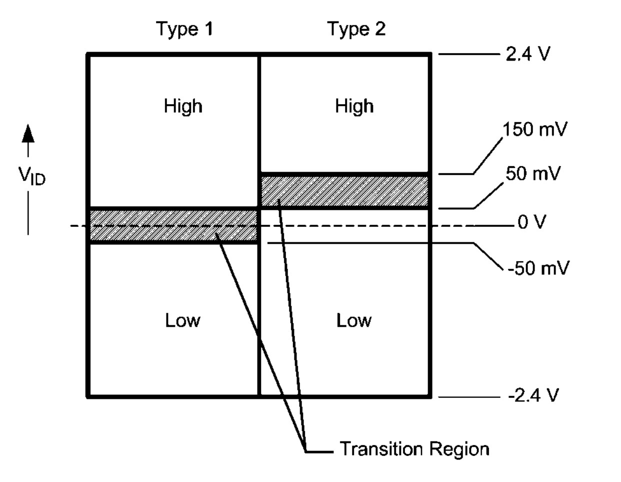


FIGURE 1. M-LVDS Receiver Input Thresholds

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	−0.3V to +4V
LVCMOS Input Voltage	−0.3V to (V_{DD} + 0.3V)
LVCMOS Output Voltage	−0.3V to (V_{DD} + 0.3V)
M-LVDS I/O Voltage	−1.9V to +5.5V
M-LVDS Output Short Circuit Current Duration	Continuous
Junction Temperature	+140°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation @ +25°C	
SQ Package	3.91W
Derate SQ Package	34 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	+29.4°C/W
θ_{JC}	+2.8°C/W
ESD Susceptibility	
HBM (Note 1)	≥8 kV
MM (Note 2)	≥250V
CDM (Note 3)	≥1250V

Note 1: Human Body Model, applicable std. JESD22-A114C

Note 2: Machine Model, applicable std. JESD22-A115-A

Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{DD}	3.0	3.3	3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	−1.4		+3.8	V
Differential Input Voltage V_{ID}			2.4	V
LVTTL Input Voltage High V_{IH}	2.0		V_{DD}	V
LVTTL Input Voltage Low V_{IL}	0		0.8	V
Operating Free Air Temperature T_A	−40	+25	+85	°C

DC Electrical Characteristics (Notes 5, 6, 7, 9)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
M-LVDS Driver							
$\|V_{AB}\|$	Differential output voltage magnitude	R_L = 50Ω, C_L = 5 pF *Figures 2, 4*		480		650	mV
ΔV_{AB}	Change in differential output voltage magnitude between logic states			−50	0	+50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	R_L = 50Ω, C_L = 5 pF *Figures 2, 3*		0.3	1.6	2.1	V
$\|\Delta V_{OS(SS)}\|$	Change in steady-state common-mode output voltage between logic states			0		+50	mV
$V_{A(OC)}$	Maximum steady-state open-circuit output voltage	*Figure 5*		0		2.4	V
$V_{B(OC)}$	Maximum steady-state open-circuit output voltage			0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output (Note 12)	R_L = 50Ω, C_L = 5pF, C_D = 0.5 pF *Figures 7, 8*				$1.2V_{SS}$	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output (Note 12)			$-0.2V_{SS}$			V
I_{IH}	High-level input current (LVTTL inputs)	V_{IH} = 3.6V		-15		15	μA
I_{IL}	Low-level input current (LVTTL inputs)	V_{IL} = 0.0V		-15		15	μA
V_{CL}	Input Clamp Voltage (LVTTL inputs)	I_{IN} = -18 mA		-1.5			V
I_{OS}	Differential short-circuit output current (Note 8)	*Figure 6*		-43		43	mA
M-LVDS Receiver							
V_{IT+}	Positive-going differential input voltage threshold	See Function Tables	Type 1		16	50	mV
			Type 2		100	150	mV
V_{IT-}	Negative-going differential input voltage threshold	See Function Tables	Type 1	−50	20		mV
			Type 2	50	94		mV
V_{OH}	High-level output voltage (LVTTL output)	I_{OH} = −8mA		2.4	2.7		V
V_{OL}	Low-level output voltage (LVTTL output)	I_{OL} = 8mA			0.28	0.4	V
I_{OZ}	TRI-STATE output current	V_O = 0V or 3.6V		−10		10	μA
I_{OSR}	Short-circuit receiver output current (LVTTL output)	V_O = 0V			-50	-90	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
M-LVDS Bus (Input and Output) Pins						
I_A	Transceiver input/output current	$V_A = 3.8V$, $V_B = 1.2V$			32	μA
		$V_A = 0V$ or $2.4V$, $V_B = 1.2V$	−20		+20	μA
		$V_A = -1.4V$, $V_B = 1.2V$	−32			μA
I_B	Transceiver input/output current	$V_B = 3.8V$, $V_A = 1.2V$			32	μA
		$V_B = 0V$ or $2.4V$, $V_A = 1.2V$	−20		+20	μA
		$V_B = -1.4V$, $V_A = 1.2V$	−32			μA
I_{AB}	Transceiver input/output differential current ($I_A - I_B$)	$V_A = V_B$, $-1.4V \le V \le 3.8V$	−4		+4	μA
$I_{A(OFF)}$	Transceiver input/output power-off current	$V_A = 3.8V$, $V_B = 1.2V$, DE = 0V $0V \le V_{DD} \le 1.5V$			32	μA
		$V_A = 0V$ or $2.4V$, $V_B = 1.2V$, DE = 0V $0V \le V_{DD} \le 1.5V$	−20		+20	μA
		$V_A = -1.4V$, $V_B = 1.2V$, DE = 0V $0V \le V_{DD} \le 1.5V$	−32			μA
$I_{B(OFF)}$	Transceiver input/output power-off current	$V_B = 3.8V$, $V_A = 1.2V$, DE = 0V $0V \le V_{DD} \le 1.5V$			32	μA
		$V_B = 0V$ or $2.4V$, $V_A = 1.2V$, DE = 0V $0V \le V_{DD} \le 1.5V$	−20		+20	μA
		$V_B = -1.4V$, $V_A = 1.2V$, DE = 0V $0V \le V_{DD} \le 1.5V$	−32			μA
$I_{AB(OFF)}$	Transceiver input/output power-off differential current ($I_{A(OFF)} - I_{B(OFF)}$)	$V_A = V_B$, $-1.4V \le V \le 3.8V$, DE = 0V $0V \le V_{DD} \le 1.5V$	−4		+4	μA
C_A	Transceiver input/output capacitance	V_{DD} = OPEN		7.8		pF
C_B	Transceiver input/output capacitance			7.8		pF
C_{AB}	Transceiver input/output differential capacitance			3		pF
$C_{A/B}$	Transceiver input/output capacitance balance (C_A/C_B)			1		
SUPPLY CURRENT (V_{CC})						
I_{CCD}	Driver Supply Current	$R_L = 50\Omega$, DE = H, $\overline{RE}$ = H		67	75	mA
I_{CCZ}	TRI-STATE Supply Current	DE = L, $\overline{RE}$ = H		22	26	mA
I_{CCR}	Receiver Supply Current	DE = L, $\overline{RE}$ = L		32	38	mA
I_{CCPD}	Power Down Supply Current	MDE = L		3	5	mA

Note 4: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 5: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 6: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.

Note 7: Typical values represent most likely parametric norms for V_{DD} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 9: C_L includes fixture capacitance and C_D includes probe capacitance.

Switching Characteristics (Notes 10, 11, 17)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AC SPECIFICATIONS						
t_{PLH}	Differential Propagation Delay Low to High	$R_L = 50\Omega$, $C_L = 5$ pF, $C_D = 0.5$ pF *Figures 7, 8*	1.5	3.3	5.5	ns
t_{PHL}	Differential Propagation Delay High to Low		1.5	3.3	5.5	ns
t_{SKD1}	Pulse Skew (Notes 12, 13)			30	125	ps
t_{SKD2}	Channel-to-Channel Skew (Notes 12, 14)			100	200	ps
t_{SKD3}	Part-to-Part Skew (Notes 12, 15)			0.8	1.6	ns
t_{SKD4}	Part-to-Part Skew (Notes 12, 16)				4	ns
t_{TLH}	Rise Time (Note 12)		1.2	2.0	3.0	ns
t_{THL}	Fall Time (Note 12)		1.2	2.0	3.0	ns
t_{PZH}	Enable Time (Z to Active High)	$R_L = 50\Omega$, $C_L = 5$ pF, $C_D = 0.5$ pF *Figures 9, 10*		7.5	11.5	ns
t_{PZL}	Enable Time (Z to Active Low)			8.0	11.5	ns
t_{PLZ}	Disable Time (Active Low to Z)			7.0	11.5	ns
t_{PHZ}	Disable Time (Active High to Z)			7.0	11.5	ns
RECEIVER AC SPECIFICATIONS						
t_{PLH}	Propagation Delay Low to High	$C_L = 15$ pF *Figures 11, 12, 13*	1.5	3.0	4.5	ns
t_{PHL}	Propagation Delay High to Low		1.5	3.1	4.5	ns
t_{SKD1A}	Pulse Skew (Receiver Type 1) (Notes 12, 13)			55	325	ps
t_{SKD1B}	Pulse Skew (Receiver Type 2) (Notes 12, 13)			475	800	ps
t_{SKD2}	Channel-to-Channel Skew (Notes 12, 14)			60	300	ps
t_{SKD3}	Part-to-Part Skew (Notes 12, 15)			0.6	1.2	ns
t_{SKD4}	Part-to-Part Skew (Note 16)				3	ns
t_{TLH}	Rise Time (Note 12)		0.3	1.1	1.6	ns
t_{THL}	Fall Time (Note 12)		0.3	0.65	1.6	ns
t_{PZH}	Enable Time (Z to Active High)	$R_L = 500\Omega$, $C_L = 15$ pF *Figures 14, 15*		3	5.5	ns
t_{PZL}	Enable Time (Z to Active Low)			3	5.5	ns
t_{PLZ}	Disable Time (Active Low to Z)			3.5	5.5	ns
t_{PHZ}	Disable Time (Active High to Z)			3.5	5.5	ns
GENERIC AC SPECIFICATIONS						
t_{WKUP}	Wake Up Time (Note 12) (Master Device Enable (MDE) time)				500	ms
f_{MAX}	Maximum Operating Frequency (Note 12)		125			MHz

Note 10: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 11: Typical values represent most likely parametric norms for $V_{DD} = +3.3V$ and $T_A = +25°C$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 12: Specification is guaranteed by characterization and is not tested in production.

Note 13: t_{SKD1}, $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 14: t_{SKD2}, Channel-to-Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.

Note 15: t_{SKD3}, Part-to-Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.

Note 16: t_{SKD4}, Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.

Note 17: C_L includes fixture capacitance and C_D includes probe capacitance.

Note 18: Measured on a clock edge with a histogram and an acummulation of 1500 histogram hits. Input stimulus jitter is subracted geometrically.

Test Circuits and Waveforms

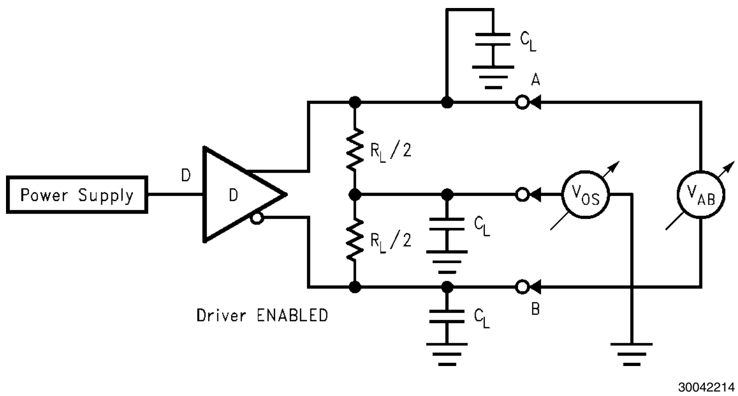


FIGURE 2. Differential Driver Test Circuit

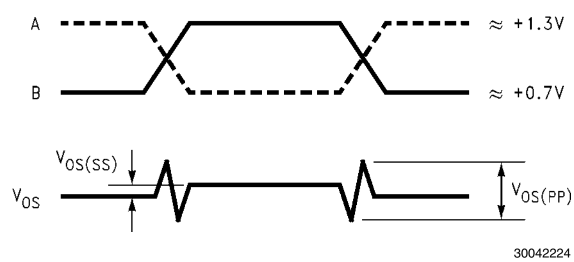


FIGURE 3. Differential Driver Waveforms

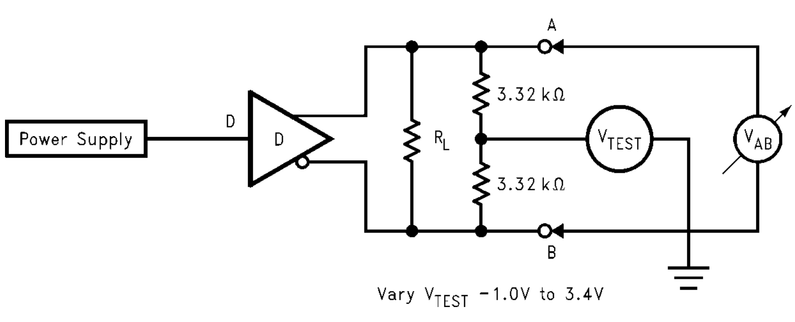


FIGURE 4. Differential Driver Full Load Test Circuit

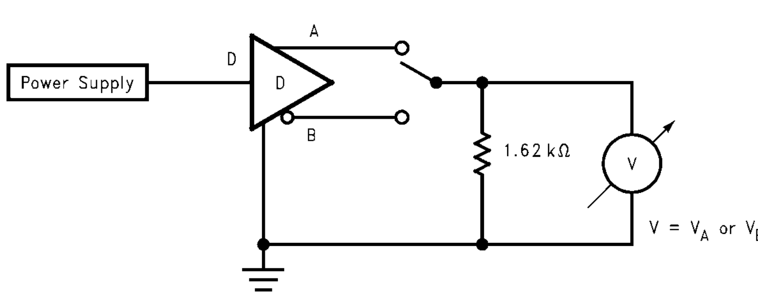


FIGURE 5. Differential Driver DC Open Test Circuit

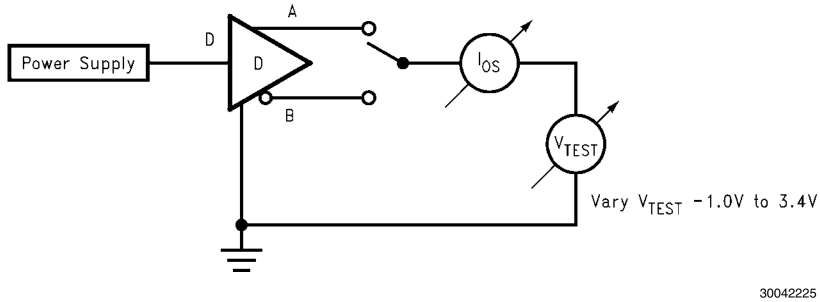


FIGURE 6. Differential Driver Short-Circuit Test Circuit

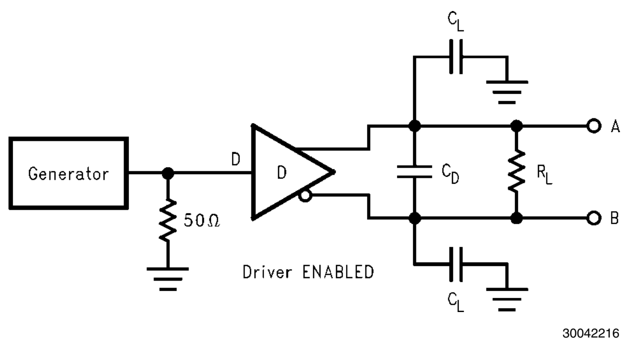


FIGURE 7. Driver Propagation Delay and Transition Time Test Circuit

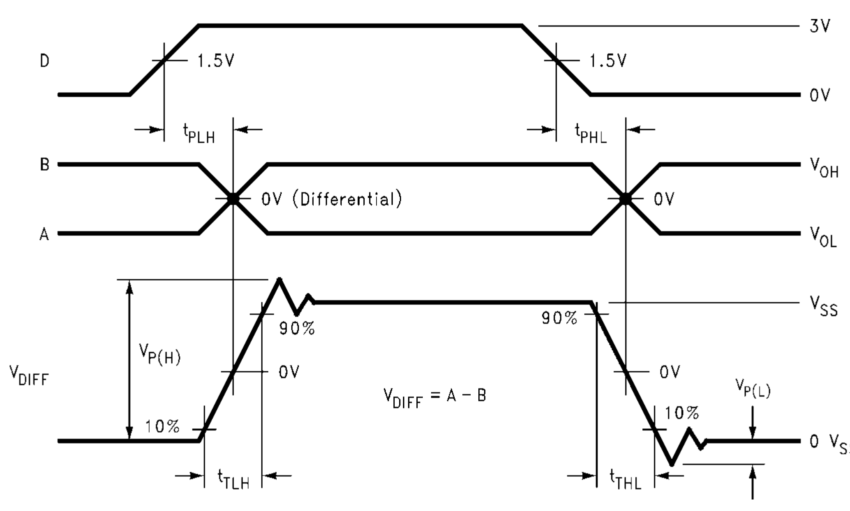


FIGURE 8. Driver Propagation Delays and Transition Time Waveforms

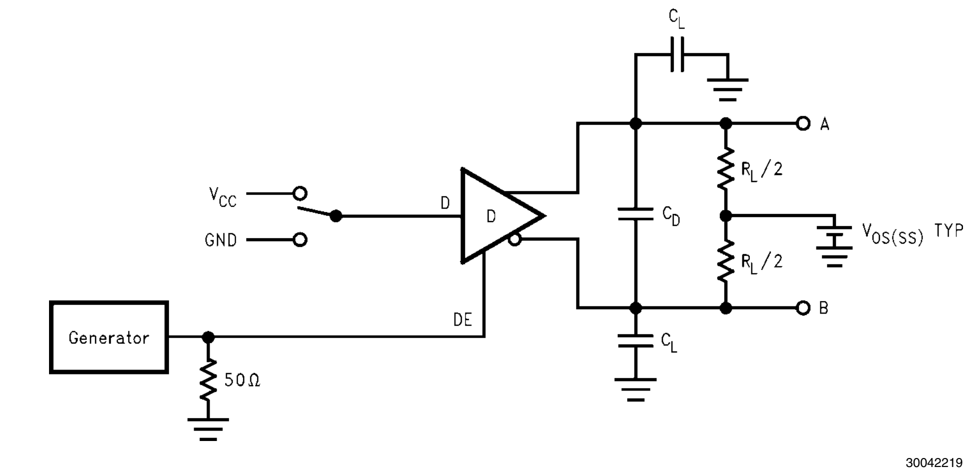


FIGURE 9. Driver TRI-STATE Delay Test Circuit

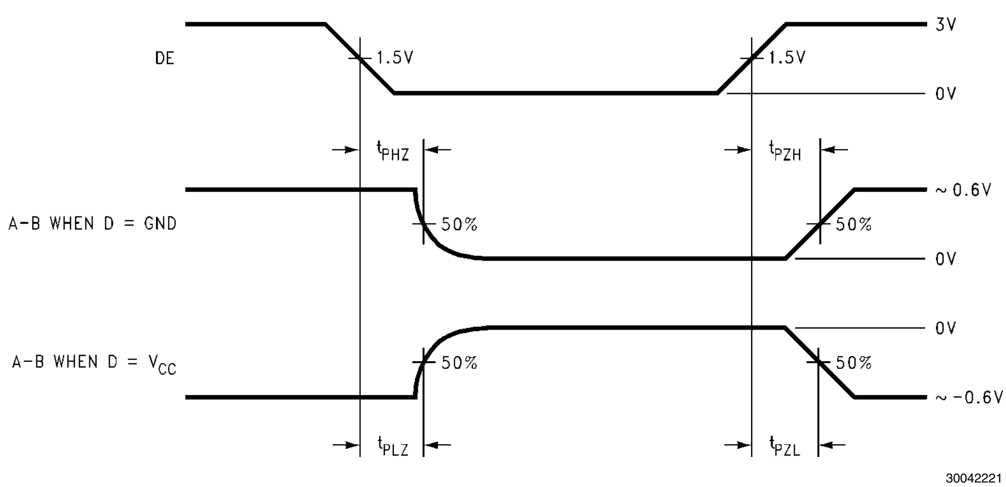


FIGURE 10. Driver TRI-STATE Delay Waveforms

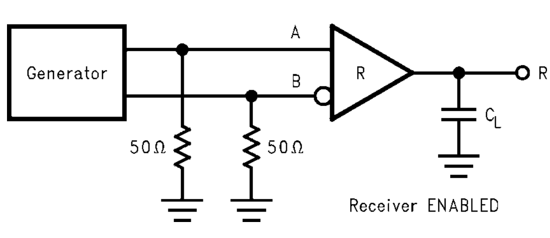


FIGURE 11. Receiver Propagation Delay and Transition Time Test Circuit

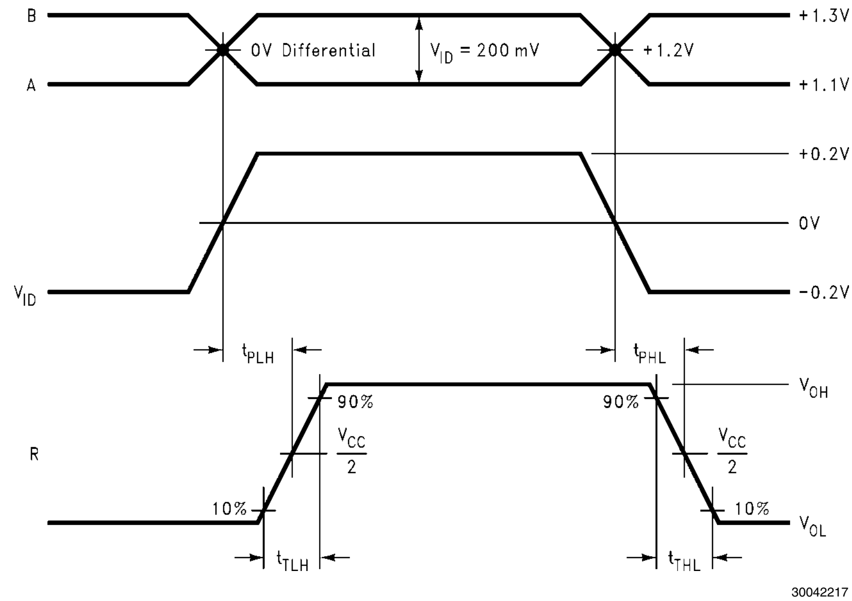


FIGURE 12. Type 1 Receiver Propagation Delay and Transition Time Waveforms

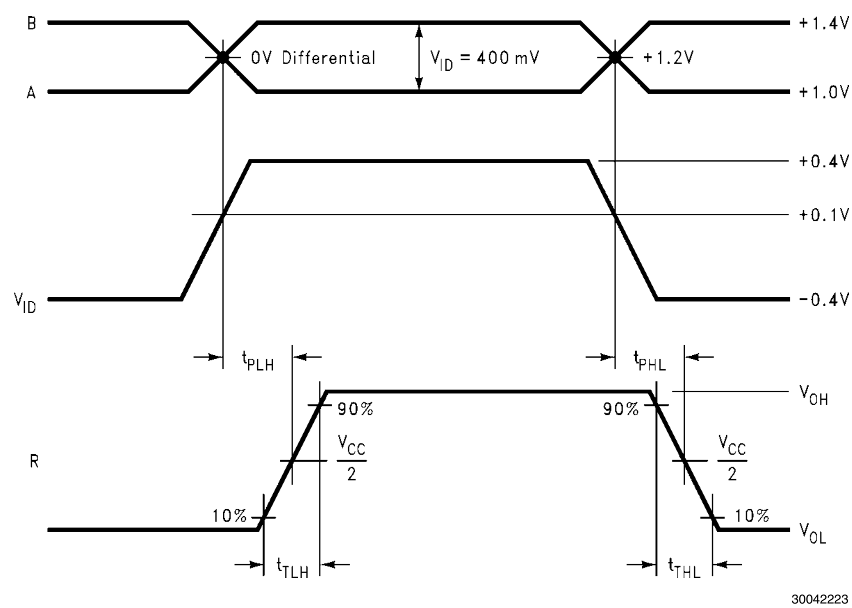


FIGURE 13. Type 2 Receiver Propagation Delay and Transition Time Waveforms

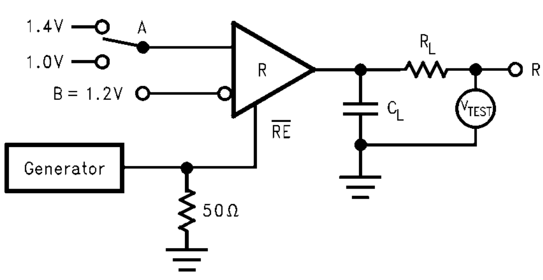


FIGURE 14. Receiver TRI-STATE Delay Test Circuit

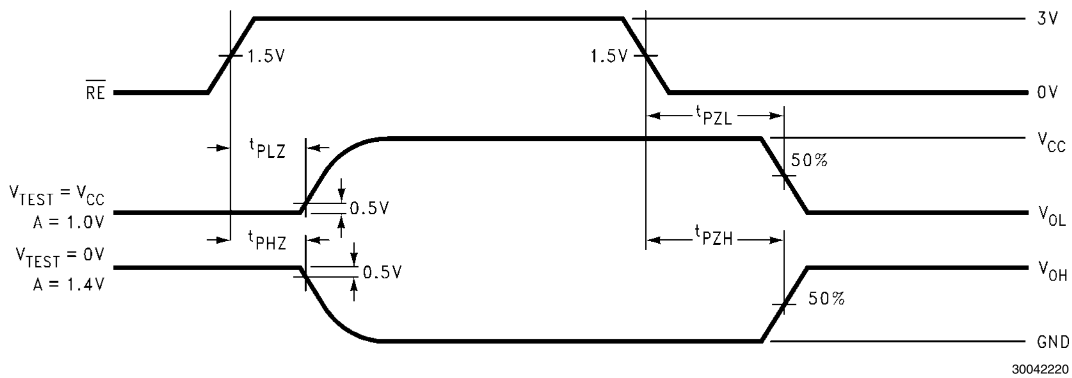


FIGURE 15. Receiver TRI-STATE Delay Waveforms

Truth Tables

DS91M040 Transmitting

Inputs			Outputs	
$\overline{RE}$	DE	DI	B	A
X	H	H	L	H
X	H	L	H	L
X	L	X	Z	Z

X — Don't care condition
Z — High impedance state

DS91M040 as Type 1 Receiving

Inputs				Output
FSEN	$\overline{RE}$	DE	A – B	RO
L	L	X	≥ +0.05V	H
L	L	X	≤ −0.05V	L
L	L	X	−0.05V ≤ A-B ≤ +0.05V	Undefined
L	H	X	X	Z

X — Don't care condition
Z — High impedance state

DS91M040 as Type 2 Receiving

Inputs				Output
FSEN	$\overline{RE}$	DE	A – B	RO
H	L	X	≥ +0.15V	H
H	L	X	≤ +0.05V	L
H	L	X	+0.05V ≤ A-B ≤ +0.15V	Undefined
H	H	X	X	Z

X — Don't care condition
Z — High impedance state

DS91M040 Type 1 Receiver Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{ICM}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	−2.400V	1.200V	L
3.800V	3.750V	0.050V	3.775V	H
3.750V	3.800V	−0.050V	3.775V	L
−1.350V	−1.400V	0.050V	−1.375V	H
−1.400V	−1.350V	−0.050V	−1.375V	L

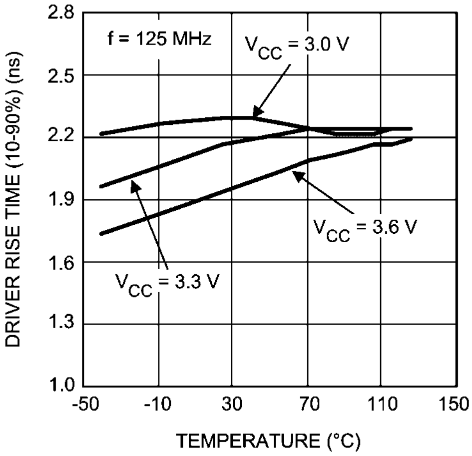
H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE}$ = L)

DS91M040 Type 2 Receiver Input Threshold Test Voltages

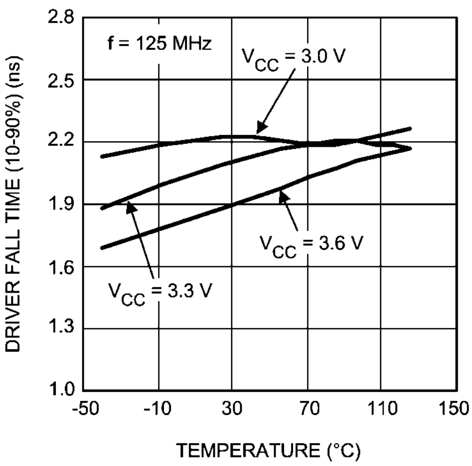
Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	−2.400V	1.200V	L
3.800V	3.650V	0.150V	3.725V	H
3.800V	3.750V	0.050V	3.775V	L
−1.250V	−1.400V	0.150V	−1.325V	H
−1.350V	−1.400V	0.050V	−1.375V	L

H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE}$ = L)

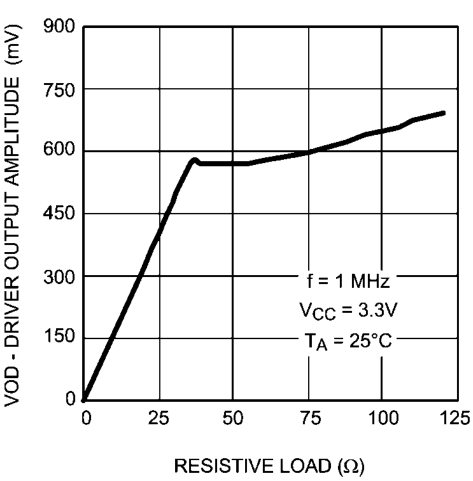
Typical Performance Characteristics



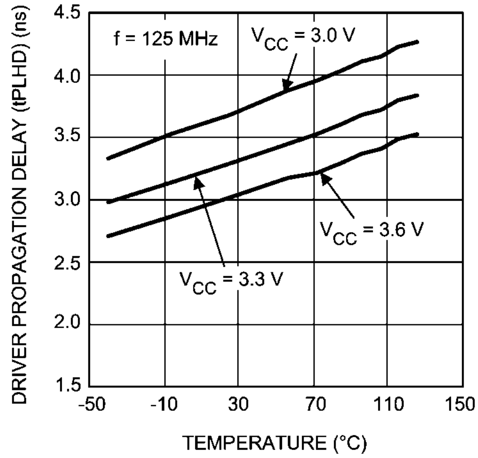
Driver Rise Time as a Function of Temperature



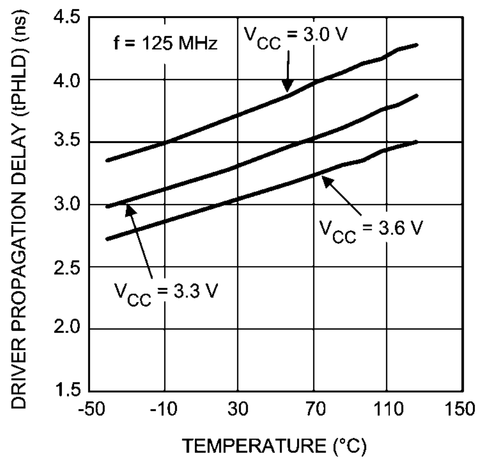
Driver Fall Time as a Function of Temperature



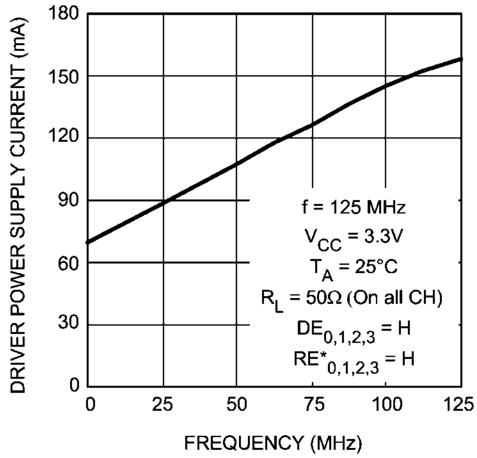
Driver Output Signal Amplitude as a Function of Resistive Load



Driver Propagation Delay (tPLHD) as a Function of Temperature



Driver Propagation Delay (tPHLD) as a Function of Temperature



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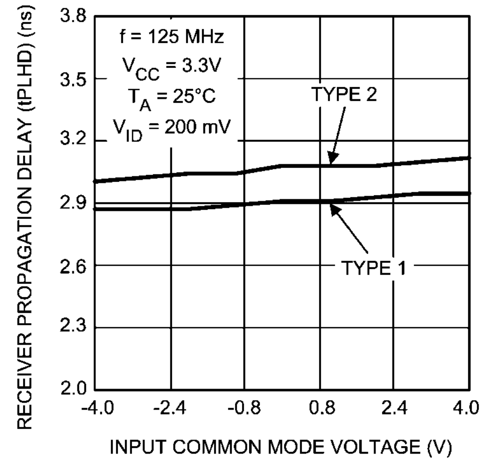
Driver Power Supply Current as a Function of Frequency



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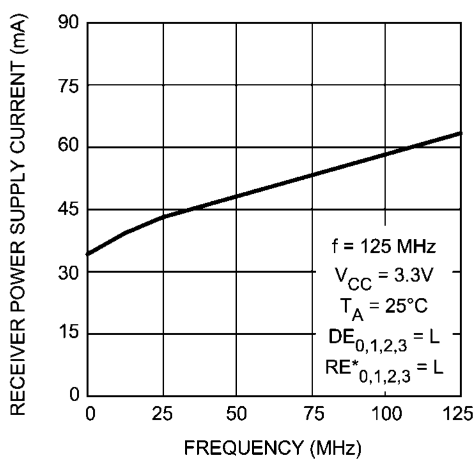
Receiver Propagation Delay (tPLHD) as a Function of Input Common Mode Voltage



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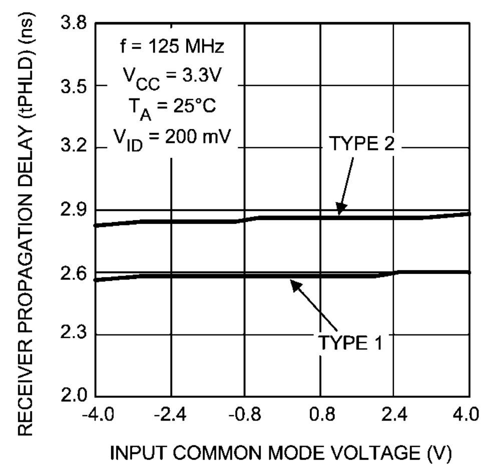
Receiver Power Supply Current as a Function of Frequency



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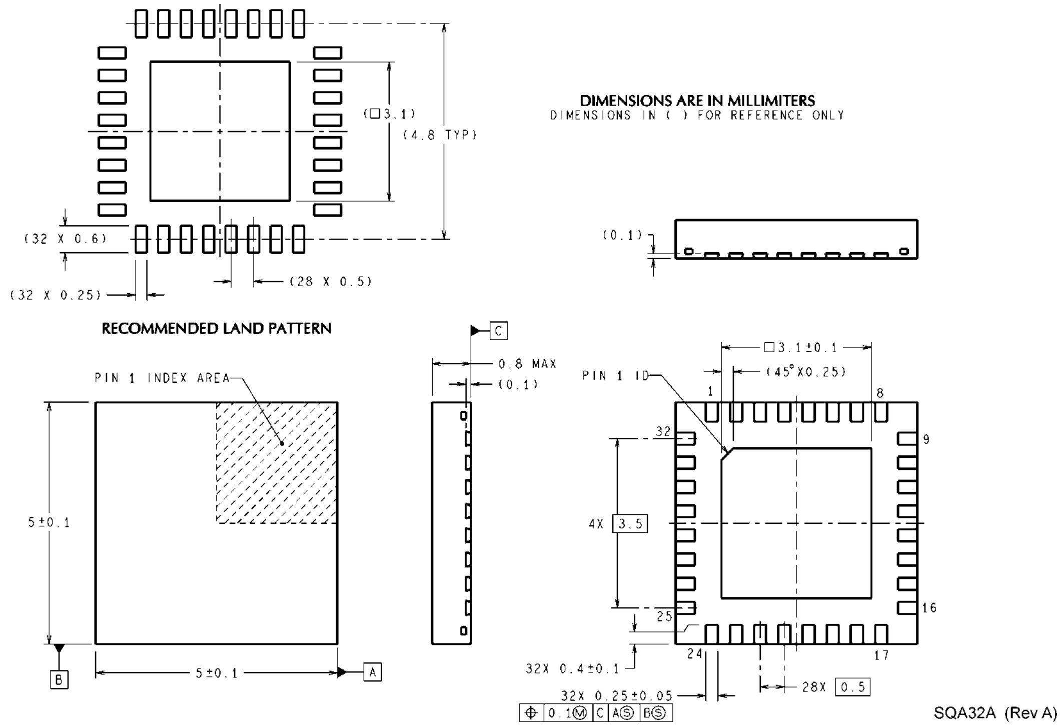
Receiver Propagation Delay (tPHLD) as a Function of Input Common Mode Voltage

Physical Dimensions inches (millimeters) unless otherwise noted



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(See AN-1187 for PCB Design and Assembly Recommendations)

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